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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,782	10/10/2003	Shin-Ae Lee	5649-1187	1793

20792 7590 05/26/2006

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,782	LEE ET AL.	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,54 and 55* is/are pending in the application.

4a) Of the above claim(s) *10 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 12, 54-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 5, 12 and 54-55 are objected to because of the following informalities:

Re claim 1, lines 2, 4-5, 6 and 8, the phrase "the gate electrode" should change to –the inverted T-shaped gate electrode--.

Re claim 1, lines 3 and 4, the phrase "the base portion" should change to –the silicon base portion.

Re claim 1, lines 4, 6, 8, the phrase "the column portion" should change to –the silicon column portion--.

Re claim 5, lines 2, 3-4 and 5, the phrase "the gate electrode" should change to –the inverted T-shaped gate electrode--.

Re claim 12, line 2, the phrase "the gate electrode" should change to –the inverted T-shaped gate electrode--.

Re claim 54, line 3, the phrase "the base portion" should change to –the silicon base portion.

Re claim 55, line 1, the phrase "the base portion" should change to –the silicon base portion.

Re claim 55, lines 1-2, the phrase "the column portion" should change to –the silicon column portion--.

Re claim 55, line 2, the phrase "the gate electrode" should change to –the inverted T-shaped gate electrode--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-4, 6-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 2, line 2, the phrase "the first and second sidewalls of the gate electrode" lacks antecedent basis (note: applicant only predefined the first and second sidewalls of the silicon column portion).

Re claim 6, line 2, the phrase "the sidewalls of the gate electrode" is unclear (i.e., sidewalls of the lateral protrusions or sidewalls of the silicon column portion or both?).

Re claim 7, the phrase "the insulating gate spacer" lacks antecedent basis.

The remaining claims 3-4 and 8 are rejected for depending from the above rejected claims.

For the purpose of patentability, these claims will be interpreted as best understood.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 5, 9 and 54-55 are rejected under 35 U.S.C. 102(b) as being anticipated by Chao, U.S./4,818,715.

Chao discloses a MOS transistor comprises an inverted T-shaped gate electrode (figs. 7d and 5e) on a substrate, the gate electrode comprising a silicon base portion and a silicon column portion extending from the base portion (figs. 7d and 5e), the base portion and the column portion doped with a same dopant material (i.e., form from the same doped layer 30, fig. 1, col. 6, lines 5-10), the base portion of the gate electrode including a first lateral protrusion extending laterally beyond a first sidewall of the column portion of the gate electrode (i.e., the column portion is right under the Si3N4) and a second lateral protrusion extending laterally beyond a second sidewall of the column portion of the gate electrode (figs. 7d and 5e); a drain region in the substrate comprising a first lightly-doped drain region n= under the first lateral protrusion (fig. 5e), a second lightly-doped drain region n- that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region (fig. 5e), and a heavily-doped drain region n-/n+ adjacent to the second lightly-doped drain region (figs. 5e and 5h); and a source region in the substrate comprising a first lightly-doped source region n= (fig. 5e, i.e., opposite to the drain region) under the second lateral protrusion, a second lightly-doped source region n- (fig. 5e) that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region, and a heavily-doped source region n-/n+ (figs. 5e and 5h) adjacent to the second lightly-doped source region; see figs. 1-11g and cols. 1-18 for more details.

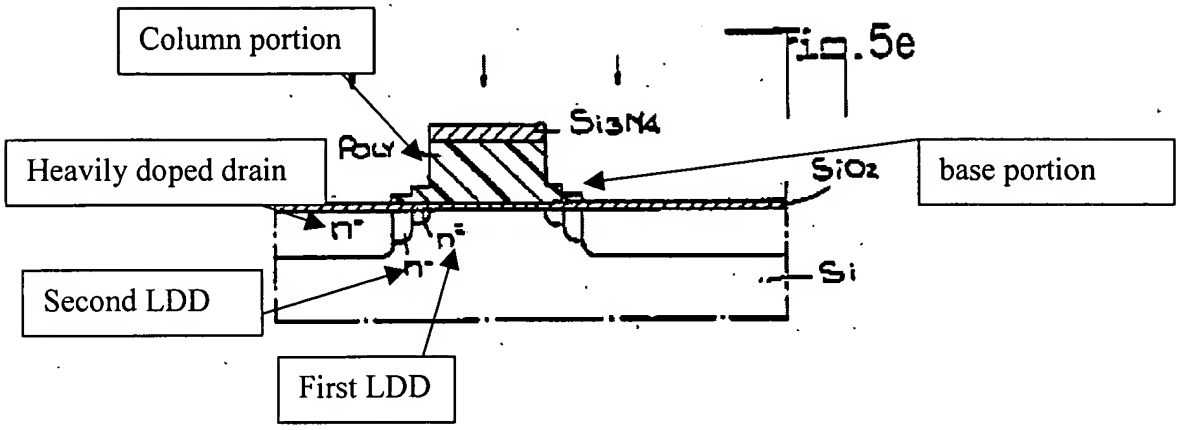

Fig. 5e

Re claim 5, further comprising a gate dielectric (SiO2, fig. 7d) interposed between the gate electrode and the substrate, wherein a first sidewall of the gate dielectric is aligned with a sidewall of the first lateral protrusion of the gate electrode (fig. 7d) and wherein a second sidewall of the gate dielectric is aligned with a sidewall of the second lateral protrusion of the gate electrode (fig. 7d).

Re claim 9, wherein the sidewalls of the first and second lateral protrusions are vertically profiled (figs. 5e and 7d).

Re claim 54, wherein the depth of the second LDD is about the same as the combined depth of the first LDD, the gate dielectric layer and the base portion of the inverted T-shaped gate electrode (figs. 5e and 7d).

Re claim 55, wherein the base portion and the column portion of the gate electrode are not selectively etchable (figs. 5e and 7d, i.e., formed from the same material).

6. Claims 1-3 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeh et al., U.S./6,008,100.

Yeh et al. discloses a MOS transistor comprises an inverted T-shaped gate electrode 106a on a substrate 100 (fig. 2F), the gate electrode comprising a silicon base portion (i.e., the slant portion) and a silicon column portion (i.e., vertical portion) extending from the base portion (fig. 2F), the base portion and the column portion doped with a same dopant material (i.e., formed from the same doped polysilicon layer 106, col. 3, lines 1-10), the base portion of the gate electrode including a first lateral protrusion extending laterally beyond a first sidewall of the column portion of the gate electrode (fig. 2F) and a second lateral protrusion extending laterally beyond a second sidewall of the column portion of the gate electrode (fig. 2F); a drain region 110a/110b/110c in the substrate comprising a first lightly-doped drain region 110a under the first lateral protrusion (fig. 2F), a second lightly-doped drain region 110b that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region (fig. 2F), and a heavily-doped drain region 110c adjacent to the second lightly-doped drain region (fig. 2F); and a source region 110a/110b/110c in the substrate comprising a first lightly-doped source region 110a under the second lateral protrusion (fig. 2F), a second lightly-doped source region 110b that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region (fig. 2F), and a heavily-doped source region 110c adjacent to the second lightly-doped source region (fig. 2F), see figs. 1-2F and cols. 1-6 for more details.

Re claim 2, further comprising an insulating gate spacer 112 (i.e., oxide, col. 3, lines 37-41) covering the first and second sidewalls of the gate electrode (fig. 2F), wherein the second lightly doped drain region and the second lightly doped source region are under bottom portions of the insulating gate spacer (fig. 2F).

Re claim 3, wherein the heavily doped drain region 110c is adjacent a first outer sidewall of the insulating gate spacer 112 (fig. 2F) and wherein the heavily doped source region 110c is adjacent a second outer sidewall of the insulating gate spacer 112 (fig. 2F).

Re claim 55, wherein the base portion and the column portion of the gate electrode are not selectively etchable (fig. 2f, i.e., since they are formed from the same material).

7. Claims 1-4, 9, 12 and 54-55 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu, U.S./5,837,588.

Wu discloses a MOS transistor comprises an inverted T-shaped gate electrode 14 on a substrate 10 (fig. 7), the gate electrode comprising a silicon base portion and a silicon column portion extending from the base portion (fig. 7 and col. 2, line 51, i.e., polysilicon 14), the base portion and the column portion doped with a same dopant material (i.e., doped during the steps of forming the source/drain region, see figs. 10 and col. 3, lines 45-65), the base portion of the gate electrode including a first lateral protrusion extending laterally beyond a first sidewall of the column portion of the gate electrode (fig. 11) and a second lateral protrusion extending laterally beyond a second sidewall of the column portion of the gate electrode (fig. 11); a drain region in the substrate comprising a first lightly-doped drain region under the first lateral protrusion (fig. 11), a second lightly-doped drain region that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region (fig. 11), and a heavily-doped drain region 9 adjacent to the second lightly-doped drain region (fig. 11); and a source region in the substrate comprising a first lightly-doped source region under the second lateral protrusion (fig. 11, i.e., opposite to the drain region), a second lightly-doped source region that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region (fig. 11), and a heavily-

doped source region 9 adjacent to the second lightly-doped source region (fig. 11), see figs. 1-11 and cols. 1-6 for more details.

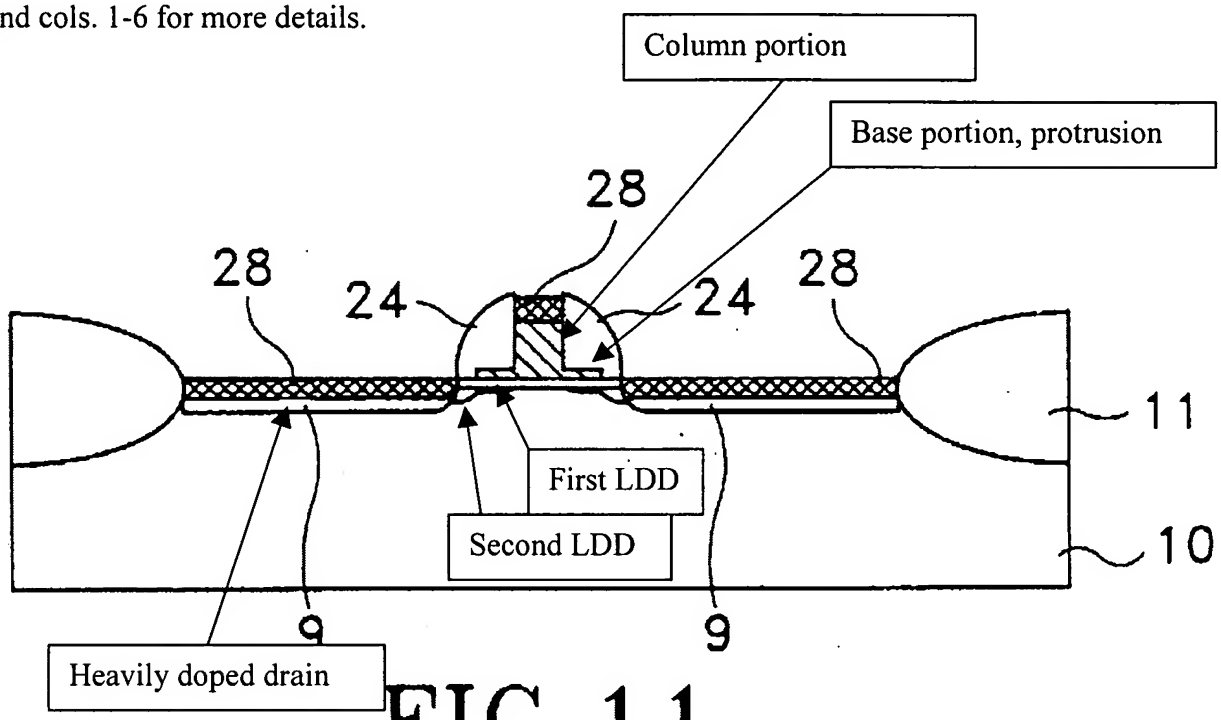

FIG. 11

Re claim 2, further comprising an insulating gate spacer 24 (i.e., oxide, col. 3, lines 34-41) covering the first and second sidewalls of the gate electrode (fig. 11), wherein the second lightly doped drain region and the second lightly doped source region are under bottom portions of the insulating gate spacer (fig. 11).

Re claim 3, wherein the heavily doped drain region 9 is adjacent a first outer sidewall of the insulating gate spacer 24 (fig. 11) and wherein the heavily doped source region 9 is adjacent a second outer sidewall of the insulating gate spacer 24 (fig. 11).

Re claim 4, wherein a bottom surface of the insulating gate spacer 24 is on a curing thermal oxide layer 12 (fig. 8).

Re claim 9, wherein the sidewalls of the first and second lateral protrusions are vertically profiled (figs. 5e and 7d).

Re claim 12, further comprising a metal silicide layer 28 on the upper surface of the gate electrode 14 (fig. 11), the surface of the heavily doped source and drain regions 9 (fig. 11).

Re claim 54, wherein the depth of the second LDD is about the same as the combined depth of the first LDD, the gate dielectric layer and the base portion of the inverted T-shaped gate electrode (fig. 11).

Re claim 55, wherein the base portion and the column portion of the gate electrode are not selectively etchable (figs. 11 since they are formed from the same material, i.e., polysilicon).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao, U.S./4,818,715 in view of Nakayama et al., U.S./6,436,776 B2.

Chao disclosed in above; however, Chao is silent to providing a curing thermal oxide layer on the sidewalls of the gate electrode, gate dielectric and the second lightly doped source/drain regions; a insulating spacer on the curing thermal oxide layer and further comprising a spacer etch stop layer interposed between the insulating gate spacer and the curing thermal oxide layer.

Nakayama et al. teaches a semiconductor device, which comprises providing a curing thermal oxide layer 207 (col. 13, lines 13-20) on the sidewalls of the gate electrode 206 (col. 12, line 66), gate dielectric 205 (col. 13, lines 1-8) and the lightly doped source/drain regions 208 (fig. 10B, col. 13, lines 14-23, called "low-concentration diffusion region"); a insulating spacer 210 (i.e., nitride, col. 13, lines 23-30) on the curing thermal oxide layer and further comprising a spacer etch stop layer 209 (i.e., SiO2, having etching selectively different from nitride, col. 13, lines 23-30) interposed between the insulating gate spacer 210 and the curing thermal oxide layer 207 (fig. 10D), see figs. 1A-12C and cols. 1-18 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further providing the curing thermal oxide layer, the spacer etch stop layer and the spacer on the sidewalls of the gate electrode, gate dielectric and the LDD regions as taught by Nakayama et al. in the device/structure of Chao in

order to eliminate the short circuit (i.e., bridging phenomenon etc.), reduce the parasitic capacitance generated between the gate electrode and the source/drain region.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed arrangement (the claimed structure Regarding claims 6-8) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

Response to Arguments

11. Applicant's arguments with respect to rejected claims have been considered but are moot in view of the new ground(s) of rejection.

With respect to the claims 10-11, these claims are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species. Should Applicants have further questions regarding the restriction matter, Applicants should file a petition.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jack Chen
Primary Examiner
Art Unit 2813

May 23, 2006